

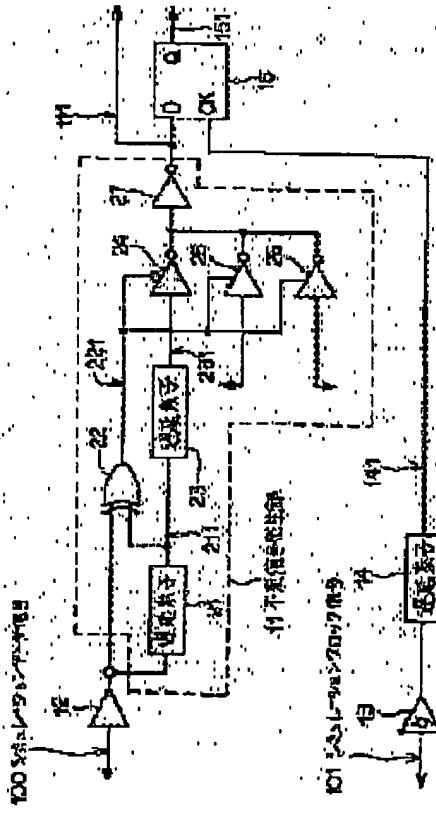
SIMULATION CIRCUIT

Patent number: JP5189517
Publication date: 1993-07-30
Inventor: ITO TOSH YUKI; MATSUMURA HIROYUKI; SATO YUICHI
Applicant: SHARP KK
Classification:
- international: G06F11/26; G06F15/60
- european:
Application number: JP19920020457 19920108
Priority number(s): JP19920020457 19920108

[Report a data error here](#)

Abstract of JP5189517

PURPOSE: To produce a test pattern in consideration of the skews caused between the tester input and output signals and also to prevent the difference of operations caused between the testers. **CONSTITUTION:** The period longer than the data set-up time set to a clock signal when a logic tester used for a real device is viewed from the outside is referred to as a 1st period. Meanwhile the period longer than the data holding time set to the clock signal is defined as a 2nd period respectively. Then the total value of the 1st and 2nd periods is defined as a 3rd period. The delay of the 1st period is given to a simulation clock signal 101 by a delay element 14. Then unfixed level, is set to a simulation data signal 100 by an unfixed signal producing part 11 in the 3rd period after an edge emerged.



Data supplied from the esp@cenet database - Worldwide